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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/829,173 | 04/22/2004 | Syotaro Ono | 252311US2S | 6045 |

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| EXAMINER | |
|---|---|
| DICKEY, THOMAS L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/829,173 | ONO ET AL. | |
| | Examiner | Art Unit | |
| | Thomas L. Dickey | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *9 and 11-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7 and 10* is/are rejected.

7)☒ Claim(s) *3 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/22/04 and 7/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

# DETAILED ACTION

## *Election/Restriction*

**1.** Applicant's election without traverse of Group II (SECOND EMBODIMENT), claims 1-8 and 10, in the Paper filed 06/20/05 is acknowledged.

## *Oath/Declaration*

**2.** The oath/declaration filed on 9/9/04 is acceptable.

## *Drawings*

**3.** The formal drawings filed on 04/22/04 are acceptable.

## *Priority*

**4.** Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

## *Information Disclosure Statement*

**5.** The Information Disclosure Statements filed on 04/22/04 AND 7/6/05 have been considered.

***Claim Rejections - 35 USC § 102***

**6.** The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**A.** Claims 1,4,5,7, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by TOKURA ET AL. (6,015,737).

Tokura et al. discloses a semiconductor device with a first semiconductor (DRAIN) region 2 of a first (N) conductivity type; a second semiconductor (BASE) region 16 of a second (P) conductivity type formed on the first semiconductor (DRAIN) region 2; a third semiconductor (SOURCE) region 4 of the first (N) conductivity type formed on a part of the second semiconductor (BASE) region 16; the first (DRAIN 2) to third (SOURCE 4) semiconductor regions being formed into a MOS field-effect transistor; a trench 50 formed to range from a surface of the third semiconductor (SOURCE) region 4 to the third semiconductor (SOURCE) region 4 and the second semiconductor (BASE) region 16, the trench 50 penetrating the third semiconductor (SOURCE) region 4, a depth of the trench 50 being shorter than a depth of a deepest bottom portion of the second semiconductor (BASE) region 16, and the trench 50 having no second semiconductor (BASE) region 16 under its bottom surface; a gate insulating film 8 formed on both facing side surfaces of the trench 50; first (part of part 9 facing left) and second (part of

part 9 facing right) gate electrodes 9, the first and second gate electrodes 9 being connected to each other at a part (part of part 9 facing down) thereof inside the trench 50, formed on the gate insulating film 8 on the respective facing side surfaces of the trench 50, the first and second gate electrodes 9 being separated from each other; and a first conductive material 18, being electrically connected to a source electrode 52 (note that source electrode 52 is formed at the same time as, and contiguous with, first conductive material 18) formed between the first and second gate electrodes 9 on the side surfaces of the trench 50, with an insulating film 18 intervened between the first conductive material 18 and the first and second gate electrodes 9, and a fifth semiconductor region 17 of the second (P) conductivity type formed on a part of the second semiconductor (BASE) region 16, the fifth semiconductor region 17 having an impurity concentration higher than an impurity concentration of the second semiconductor (BASE) region 16; wherein the source electrode 52 is formed on the fifth semiconductor region 17 and the third semiconductor (SOURCE) region 4. Note figure 22 and column 13 lines 32-55 of Tokura et al.

**B.** Claims 1,6, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by BABA ET AL. (5,126,807).

Baba et al. discloses a semiconductor device with a first semiconductor (DRAIN) region 3 of a first (N) conductivity type; a second semiconductor (BASE) region 5 of a second (P) conductivity type formed on the first semiconductor (DRAIN) region 3; a third semiconductor (SOURCE) region 7 of the first (N) conductivity type formed on a part of

the second semiconductor (BASE) region 5; the first (DRAIN 3) to third (SOURCE 7) semiconductor regions being formed into a MOS field-effect transistor; a trench 23 formed to range from a surface of the third semiconductor (SOURCE) region 7 to the third semiconductor (SOURCE) region 7 and the second semiconductor (BASE) region 5, the trench 23 penetrating the third semiconductor (SOURCE) region 7, a depth of the trench 23 being shorter than a depth of a deepest bottom portion of the second semiconductor (BASE) region 5, and the trench 23 having no second semiconductor (BASE) region 5 under its bottom surface; a gate insulating film 9 formed on both facing side surfaces of the trench 23; first and second gate electrodes 17 formed on the gate insulating film 9 on the respective facing side surfaces of the trench 23, the first and second gate electrodes 17 being separated from each other; and a first conductive material 11, being a floating electrode, formed between the first and second gate electrodes 17 on the side surfaces of the trench 23, with an insulating film 13 intervened between the first conductive material 11 and the first and second gate electrodes 17.

Note figure 5, column 4 lines 51-68, and column 5 lines 1-5 and 19-24 of Baba et al.

***Claim Rejections - 35 USC § 103***

**7.** The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**A.** Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over TOKURA ET AL. (6,015,737) in view of SUZUKI ET AL. (JP-2000269487).

Tokura et al. discloses a semiconductor device with all the limitations of claim 2 except a fourth semiconductor region of the first conductivity type formed between the bottom surface of the trench and the first semiconductor (DRAIN) region, the fourth semiconductor region having an impurity concentration higher than an impurity concentration of the first semiconductor (DRAIN) region. Note figure 22 and column 13 lines 32-55 of Tokura et al.

However, Suzuki et al. discloses a semiconductor device with a fourth semiconductor region 32 of the first (N) conductivity type formed between a bottom surface 30A of a trench 30 and a first semiconductor (DRAIN) region 4, the fourth semiconductor region 32 having an impurity concentration (note paragraph 0031) higher than an impurity concentration of the first semiconductor (DRAIN) region 4. Note figure 2 and paragraphs 0029-0037 of Suzuki et al. Suzuki et al. teach that this region 32 serves as a current path between a channel field 6a and Suzuki et al.'s first semiconductor (DRAIN) region 4 the ON time of the device, which provides low resistance. Therefore, it would have been obvious to a person having skill in the art to augment Tokura et al.'s semiconductor device with the fourth semiconductor region of the first conductivity type formed between the bottom surface of a trench and a first semiconductor (DRAIN) region, the fourth semiconductor region having an impurity concentration higher than an impurity concentration of a first semiconductor (DRAIN)

region such as taught by Suzuki et al. in order to a provide a current path between a channel field and the first semiconductor (DRAIN) region to thus provide lower ON resistance.

***Allowable Subject Matter***

**8.** Claims 3 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

**9.** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Thomas L. Dickey**
**Patent Examiner**
**Art Unit 2826**
**07/05**

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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